Kindly **add** the following claims:

151. A method of operating a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising:

providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read or write request; and

issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to an external clock signal.

152. The method of claim 151 further including providing a first write request to the memory device wherein, in response to the first write request, the memory device inputs the first amount of data corresponding to the first block size information from the bus synchronously with respect to the external clock signal.

153. The method of claim 152 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be input from the bus in response to a write request; and

issuing the second write request to the memory device, wherein in response to the second write request, the memory device inputs the amount of data corresponding to the second block size information from the bus synchronously with respect to the external clock signal.

154. The method of claim 152 wherein the first block size information and the first write request are included in a request packet.

155. The method of claim 154 wherein the first block size information and the first write request are included in the same request packet.

156. The method of claim 151 further including issuing a second read request to the memory device, wherein in response to the second read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to the external clock signal.

157. The method of claim 156 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be output onto the bus in response to a read request; and

issuing a third read request to the memory device, wherein in response to the third read request, the memory device outputs the

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second amount of data corresponding to the second block size information onto the bus synchronously with respect to the external clock signal.

158. The method of claim 151 further including providing a code which is representative of a delay time to transpire before data is output onto the bus after receipt of a read request, wherein the memory device stores the code in an access time register on the memory device.

159. The method of claim 158 further including receiving the external clock signal wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time.

160. The method of claim 158 wherein the code represents a number of cycles of the external clock and wherein the number of cycles is a fraction or a whole number.

161. The method of claim 151 wherein the first block size information and the first read request are included in a request packet.

162. The method of claim 161 wherein the first block size information and the first read request are included in the same request packet.

163. The method of claim 151 wherein the first block size information is a binary representation of the amount of data to be output after receipt of the first read request.

164. The method of claim 151 wherein the first block size information is indicative of an amount of data corresponding to a page mode access.

165. The method of claim 151 wherein the external clock signal has a fixed frequency and wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles of the external clock signal.

166. The method of claim 151 further including generating at least one internal clock signal using the external clock signal wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.

167. The method of claim 166 wherein the internal clock signal is generated by a delay locked loop.

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168. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method comprising:

receiving first block size information, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read or write request;

receiving a first read request; and

outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to an external clock signal.

169. The method of claim 168 further including:

receiving a second read request, and

outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the external clock signal.

170. The method of claim 168 further including:

receiving a first write request, and

inputting the first amount of data corresponding to the first block size information, in response to the first write request, from the bus synchronously with respect to the external clock signal.

171. The method of claim 170 further including:

receiving second block size information, wherein the second block size information defines a second amount of data to be input from the bus in response to a write request; and

receiving the second write request;

inputting the amount of data corresponding to the second block size information, in response to the second write request, from the bus synchronously with respect to the external clock signal.

172. The method of claim 170 wherein the first block size information and the first write request are included in a request packet.

173. The method of claim 172 wherein the first block size information and the first write request are included in the same request packet.

174. The method of claim 168 further including storing a delay time code in an access time register, the delay time code being representative of a number of clock cycles to transpire before data is output onto the bus after receipt of a read request and wherein the first amount of data corresponding to the first block size information is output in accordance with the delay time code.

175. The method of claim 174 wherein the delay time code is stored in the access time register after power is applied to the memory device.

176. The method of claim 175 wherein the number of clock cycles is a fraction or a whole number.

177. The method of claim 168 wherein the first block size information and the first read request are included in a request packet.

178. The method of claim 177 wherein the first block size information and the first read request are included in the same request packet.

179. The method of claim 168 wherein the first block size information is a binary representation of the first amount of data to be output after receipt of the first read request.

180. The method of claim 168 wherein the first block size information is indicative of an amount of data corresponding to one of a plurality of page mode accesses.

181. The method of claim 168 wherein the external clock signal has a fixed frequency and wherein the first amount of data corresponding to the first block size information is output synchronously during a plurality of clock cycles of the external clock signal.

182. The method of claim 181 further including automatically precharging the synchronous memory device after executing the first read request.

183. The method of claim 168 further including generating at least one internal clock signal using a delay locked loop and the external clock signal wherein the first amount of data corresponding to the first block size information is output onto the bus synchronously with respect to at least one internal clock signal.

184. A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells and a time delay register, the method comprises:

storing a value in the time delay register, the value being representative of a number of external clock cycles after which the memory device responds to a read request;

receiving an external clock signal wherein the external clock signal has a fixed frequency;

receiving block size information, wherein the block size information defines a first amount of data to be output onto the bus in response to a read request;

receiving a first read request;

outputting the first amount of data corresponding to the block size information onto the bus in response to the first read request;

receiving a second read request;

outputting the first amount of data corresponding to the block size information onto the bus in response to the second read request; and